High-Speed Low-Power Low Voltage CMOS Level Converter

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Abstract

The level converter is an important component in Multiple Supply Voltage (MSV) circuits. In CMOS logic, the conversion of signal from lower voltage level to higher one requires special circuitry. In this paper, we propose a level converter circuit, which provides both fast voltage level shifting and lower power consumption. Based on the HSPICE simulation and evaluation of the proposed circuit, the power consumption is reduced by more than 100% and speed up to 90% compared with Dual Cascode Voltage Switch (DCVS), and the proposed circuit can operate from 1.2V shift to 5V level. The proposed circuit is crucial_for high-speed low-power applications, such as MSV systems and IO buffer.

Key words : Level converter, Dual cascode voltage switch, Multiple supply voltage

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Introduction

Recently, the power consumption has becoming an important issue on portable electronic systems. In static CMOS circuits, it is well known that power consumption is dominated by the dynamic power consumption, which is proportional to the square of supply voltage. With its quadratic relationship to power, lowering voltage offers the most effective way of reducing power consumption [1]. However, the penalty of lowering voltage is increased propagation delay time proportional to $V_{DD}/(V_{DD}-V_T)^2$, where V_T is the transistor threshold voltage [2].

To achieve high-speed and low-power consumption, the MSV scheme has been used to design high performance chip [2]-[5]. This scheme has the advantage that those gates in non-critical paths operated at the "low" voltage level, "VDDL", while the "high" supply voltage, VDDH, is still applied for those gates in critical paths. Meanwhile, the circuit's speed can never be degraded, but the power consumption may be reduced effectively. To adjust the signal voltage level, it is necessary to insert level converters between these two kinds of gates. However, signal conversion as well as multiple supply voltages will result in increasing the overall system cost and complexity. Hence, the level converting must be accomplished with minimal delay and lower power consumption to achieve high performance CMOS circuits.

In this paper, we propose a level converter circuit, which will provide a fast voltage level shifting and reduce the power consumption of a datapath design through use of MSV. The simulation results showed both speed and power consumption of the proposed circuit are superior to those of DCVS.

Voltage Level Shifting

Due to the PMOS transistor will not turn off while VDDH – VDDL > Vtp [6], there exists a severe problem in converting a signal from "low" to "high". In general, it is practical to place a voltage level converter on each signal path, which connects the lower supply voltage cells to the higher supply voltage cells. Moreover, the level converters need both of the voltage supplies of the VDDH and the VDDL, it is also an important issue to reduce the power consumption of level converters. Fig.1 shows a popular level converter, named the Dual Cascode Voltage Switch (DCVS). This conventional level converter has relatively large delay because it is rely on a contention between different transistors on the level shifting path [6]. For example, there is a contention at node Q and node QB between the pull-down transistors (MN1 and MN2) and the pull-up transistors (MP1 and MP2). This contention problem will lead to increase both delay time and power consumption. Hence, we propose an improved circuit, named the Cross-Coupled DCVS (CCDCVS) circuit, to minimize the contention problem.

The Proposed Level Converter Circuit

The proposed level converter architecture reducing the contention problem can achieve high speed and low power consumption. The configuration is shown in Fig.2. In this circuit, we add two NMOS (MN3 and MN4) transistors to improve the DCVS circuit. There are two phases to analysis. In the first phase, set input signal IN = 0, the MN2 transistor will turn on by node B and MN1 transistor will turn off by node A respectively, and the node B charge the node QB and node A discharge the node Q simultaneously. These results lead to pull-down the node Q and pull-up the node QB efficient. In the second phase, set input signal IN = 1, it is reverse operation for first phase.

Clearly, there are three paths to speedup the output level transition in each phase, it can reduce contention problem on nodes Q and QB. In order to charge the

nodes Q and QB, the inverters I2 and I3 are larger size to increase charge and discharge capacity, and additional inverter I4 to addition output driving ability.

The Simulation Results and Comparisons

Circuit simulation was carried out using HSPICE and 0.35 μ m CMOS technology parameters on a SUN ULTRA 10 workstation. Input signals were applied through an inverter since the output waveform of an inverter will be a more realistic signal in an actual design. Spice waveforms of the proposed level converter and DCVS are shown in Fig.3 for VDDH=5V, VDDL=1.5V and an output capacitance of 0.1 pF. The summary results are listed in Table I.

In the simulation and results, the proposed level converter circuit speed fast about 90% and power saving about 100% than DCVS circuit. Furthermore, the simulation results show that the proposed level converter can operate voltage level from 1.2V shift to 5V is better than DCVS circuit.

Conclusion

In this paper, we propose a high-speed low-power level converter circuit. To reduce contention problem, we add two NMOS transistors to appropriate site and scale up the input buffer to achieve high performance issue. Our simulation results reveal that the proposed circuit has faster speed and lower power consumption compared with the DCVS circuit. Additionally the proposed circuit can operate level range from 1.2V shift to 5V, this feature is useful on the more low voltage supply systems. It was shown that the proposed level converter circuit can achieve very high speeds at a much lower power than the existing level converter circuit.

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Table I: A comparison of two level converters

Converter Schematic	VDDL (V)	VDDH (V)	Rise Time (nS)	Fall Time (nS)	Power Consumption (μW)
DCVS	3.3	3.3	0.89	0.76	96
	1.8	3.3	1.35	1.12	115
	1.5	3.3	2.26	2.18	170
	1.5	**5**	**3.26**	**4.37**	**716**
	1.2	5	--	--	--
CCDCVS	3.3	3.3	1.02	0.75	82
	1.8	3.3	1.35	1.07	93
	1.5	3.3	1.74	1.47	103
	1.5	**5**	**1.86**	**1.66**	**324**
	1.2	5	4.55	4.74	679

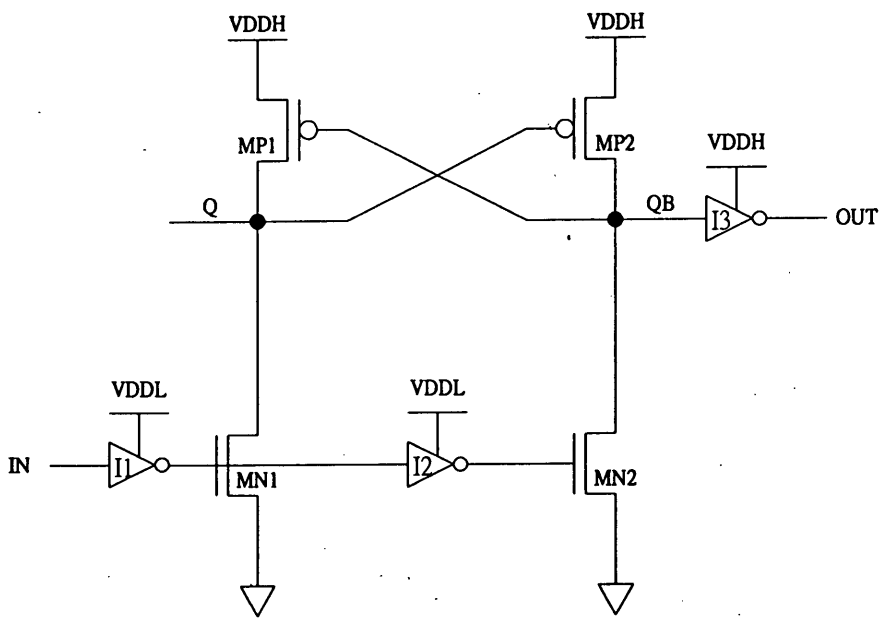

Fig.1 DCVS level converter

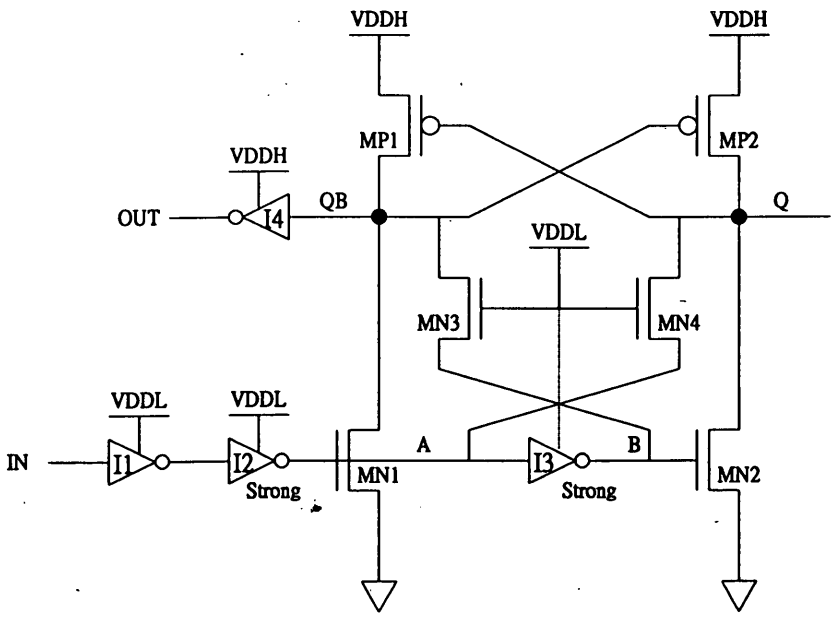

Fig.2 The proposed level converter (CCDCVS)

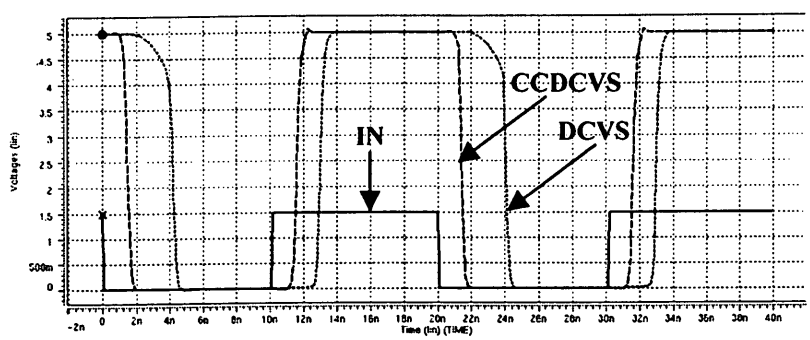

Fig.3 HSPICE simulation with DCVS and CCDCVS level converter

具高速-低功率損耗-低電壓之 CMOS 位準轉換器設計

余 建 政

摘 要

在多供應電壓(MSV)電路中，位準轉換器佔很重要的地位。CMOS 邏輯電路中，需要特別的電路將低位準電壓轉換成高位準電壓。本文中，我們提出具低電壓、低功率消耗的位準轉換器；同時，我們和傳統的位準轉換電路 DCVS 做比較。經由 HSPICE 模擬數據可知：我們所提出的電路比傳統的位準轉換電路加快 90%的速度且減少 100%的功率損耗。因此，我們所提出的電路適合使用在 MSV、IO 緩衝器等高速、低功率消耗的應用上。

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