A Power-Saving CMOS Level Converter for Dual Supply Voltages

Chien-Cheng Yu

Abstract

When using dual supply voltages, the circuit requires level converters at the interface of V_{DDH} and V_{DDL} gates to block the static current which occurs if a V_{DDL} gate drives a V_{DDH} gate. In this paper, a Power-Saving level converter (PSLC) is proposed which has the advantages of low power consumption and high operating speed, and it may operate at different values of V_{DDL} ranging from 1.2V to 4.2V. These level converters are simulated for different capacitive loads and operating supply voltage levels using the HSPICE parameters of a 0.35 μm digital CMOS technology. HSPICE simulation results show that an average power saving of 50% and 60% speed increase can be obtained compared to those of the existing technique. Hence, the proposed technique is suited for low power design without degrading performance.

Key words: Power saving, Level converter, contention

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1. Introduction

Recently, requirements for faster operating speeds and reduced power consumption, especially for portable equipment such as notebook computers, will force still further advances on circuit design technologies. One benefit of CMOS technology is that it reduces the problem of power consumption and increases packing density in an integrated circuit. In static CMOS circuits, it is well known that power consumption is dominated by the dynamic power consumption, which is proportional to the square of supply voltage. With its quadratic relationship to power, lowering voltage offers the most effective way of reducing power consumption. However, reducing the supply voltage comes at the cost of increased gate delays and therefore lower functional performance [1]. With the above observation, many researchers have reported on the techniques in which the supply voltage V_{DD} is reduced without degrading the performance [2]-[7].

More recently, the use of Multiple Supply Voltage (MSV) on the chip is becoming common place. This scheme has the advantage of allowing those gates on the critical paths to use the higher supply voltage V_{DDH}, while allowing those gates on the non-critical paths operate at the lower supply voltage V_{DDL}. However, it should be noted that when the output of a V_{DDL} circuit is connected to the input of a V_{DDH} circuit, there exists a static current flowing directly from the applied voltage source to ground, which will consume more power than is necessary. For this scheme to work well, we will however need to insert level converters between connected blocks that operate at different supply voltage levels. In addition, a structure with more low-to-high voltage blocks will need several of level converters to be inserted at each low-to-high interface [5]. Since a level converter generates the additional delay and dynamic power to the circuit, the number of level converters should be minimized and the power consumption of these level converters must be taken into account to reach high performance CMOS circuits. The emphasis of this paper is on minimizing the power consumption in level

converters.

In the traditional level converter, called Dual Cascode Voltage Switch (DCVS), there exists a drawback that this one has relatively large delay because it is rely on a contention between different transistors on the level shifting path [6]. This contention problem will result in increasing both delay time and power consumption. In this paper, we propose an improved circuit, named Power-Saving level converter (PSLC) circuit to reduce the contention problem so that it can decrease both delay time and power consumption. In comparison with the existing circuit technique, the results clearly show that the proposed circuit has the superior power-delay performance.

The remainder of this paper is orgnized as follows. Section II presents a brief description of the existing level converter. The circuit performance of the proposed adder is compared with the existing level converter in terms of power and delay, which are discuss in section III. Last section is a conclusion and summary for this paper.

2. The Existing Level Converter Circuit

A. Voltage Level Shifting

Usami and Horowitz [7] proposed a technique to reduce the power consumption in a circuit by making use of two supply voltage levels. This approach has the advantage that those gates on the critical paths can keep operating at the original voltage level for maintaining the circuit timing performance, while the ones on the non-critical paths can operate at the lower supply voltage for reducing the power consumption. However, situations often arise when the output of the V_{DDL} circuit is directly connected to the input of the V_{DDH} circuit, as shown in Fig. 1. If the input node N1 of the V_{DDL} circuit swings from high to low, the output node N2 then goes to high, that is V_{DDL}. Subsequently, the logical high at node N2 should turn off the pull-up transistor MP1 and turn on the pull-down transistor MN1. Although the voltage at node N2 is high enough to activate the NMOS transistor

MN1, it cannot turn off the PMOS transistor MP1 due to the fact that $V_{DDL}<V_{DDH}-|V_{th,p}|$. Therefore, there exists a static current flowing directly from the applied voltage source to ground via the path of MP1 and MN1, which also consumes power what is not desirable for low power design.

To avoid this undesirable power consumption, when using dual supply voltages, the circuit requires level converters at the interface of V_{DDH} and V_{DDL} gates to block the static current which occurs if a V_{DDL} gate drives a V_{DDH} gate. It is clear that no level converter is needed when the output of a V_{DDH} circuit is connected to the input of a V_{DDL} circuit. Hence, the level conversion must be accomplished with minimal delay and lower power consumption to achieve high performance CMOS circuits.

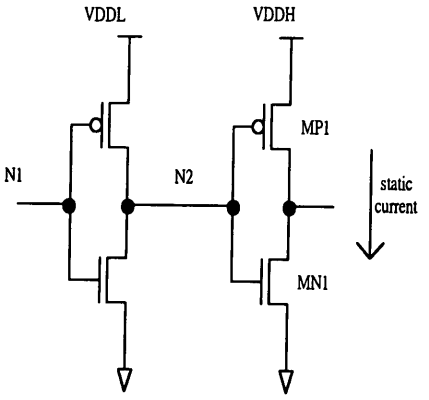

Fig.1 Direct connection of V_{DDL} circuit and the V_{DDH} circuit

B. The Existing Level Converter Circuit

Fig.2 shows the traditional level converter circuit, named Dual Cascode Voltage Switch (DCVS). In this circuit, there are two cross-coupled PMOS transistors MP1 and MP2 to form the circuit load. The cross-coupled PMOS transistors act as a differential pair. Thus, when the output at one side gets pulled low, then the opposite P transistor will be turned on, and the output on that side will be pulled high. Below the PMOS load, there are two NMOS transistors MN1 and MN2 that controlled by

the input signal IN.

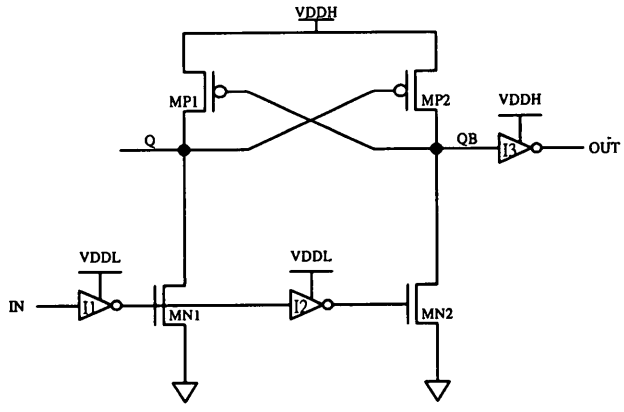

Fig.2 The DCVS level converter

Let us assume that initially the input signal IN is given by logic low so that MN2 is in cutoff while MN1 is biased active and provides a conducting path to ground. This will pull the node Q down to ground, which in turn bias MP2 into conduction. When the input signal IN is switched to logic high, the operation is forced to reverse states.

3. The Proposed Level Converter Circuit

The proposed level converter circuit (PSLC), shown in Fig. 3, employs a pair of PMOS transistors (MP3 and MP4) to form a cross-latch circuit. In this circuit, both the cross-latch PMOS transistors are added as the pull-up device. The output inverter is used to increase the driving capability of this circuit and restore the output logic swing voltage. The gates of the PMOS transistors MP3 and MP4 are connected to the output nodes QB and Q, respectively. Obviously, if the nodes Q and QB can be transferred state quickly, it will improve the short circuit power consumption. These two NMOS transistors are placed below the cross-latch PMOS transistors to cut off the static current path after evaluation. In order to determine the driving capability, an additional capacitor is connected to the output end of each circuit. Then the driving capability can be reflected by its rising and falling time. In addition,

input signal was applied through an inverter since the output waveform of an inverter will be a more realistic signal in an actual design.

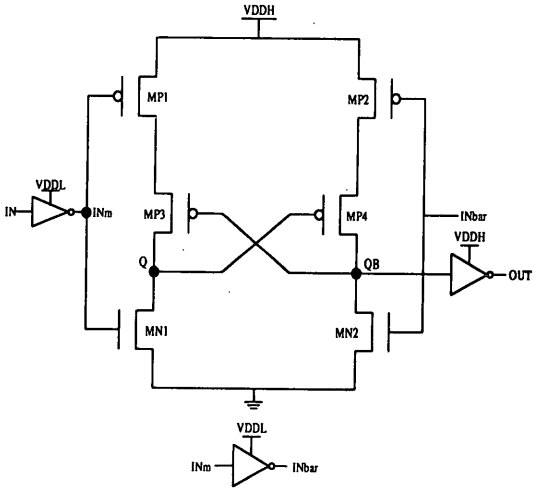

Fig.3 The proposed level converter (PSLC)

To analyze this circuit, we consider the both conditions of input signal IN. First, when input signal IN=0 and INb=1, PMOS transistor MP2 and NMOS transistor MN1 will be turned on and PMOS transistor MP1, NMOS MN2 are turned off. The node Q is then discharged to the ground. The ground level on the node Q turns the cross-latch PMOS transistor MP4 on. Then, the node QB starts to be charged to high by PMOS transistors MP2 and MP4. At this moment, due to the gate voltage of PMOS transistor MP3 is controlled by the node QB and keeps in high level at the end of the operation. On the other hand, when the input signal IN=1 and INb=0, PMOS transistor MP1 and NMOS transistor MN2 will be turned on and PMOS transistor MP1, NMOS transistor MN2 are turned off. The node QB is then discharged to the ground. The ground level on the node QB turns the cross-latch PMOS transistor MP3 on. The node Q will then be charged to high. This is an improvement over the DCVS circuit, where the pull-up and pull-down are in contention between nodes Q and QB.

4. Simulation Results and Comparisons

The DCVS and PSLC circuits are simulated for different operating voltage levels

and capacitive loads using the HSPICE parameters of a 0.35 μm digital CMOS technology. Table I. compares the output rise time, output fall time and power consumption of Figs. 2-3. The results in Table I are obtained from HSPICE simulations using 0.1pF capacitive load. From Table I, we can see that the rising time and falling time of the PSLC circuit are shorter than the ones in DCVS circuit at each capacitive load. Unlike a typical CMOS gate that has reduced static power consumption with increased capacitive load, the PSLC has increases in power consumption with increasing capacitive loads. This is because the PMOS transistor MP2 takes more time to turn off with increasing capacitive load.

From the analysis of these HSPICE simulation results, an additional 50% power reduction and 60% speed increase over those of the DCVS technique at V_{DDH}=5V, V_{DDL}=1.5V with output capacitive load = 0.1pF are achieved. It is evident the proposed method has better performance than the existing method, with respect to the operating speed and the power consumption. In addition, it can be seen that the proposed level converter can operate at different values of V_{DDL} ranging from 1.2V to 4.2V.

5. Conclusion

In this paper, we propose a new low-power level converter circuit (PSLC) which has the advantages of fast speed and low power with signal buffering between stages. The buffering inverters not only restore the output signals to the supply voltages, but also are flexible in sizes to accommodate the different loading from interconnections and fan-outs. These characteristics provide significant leverage in our design. The proposed circuit will reduce the contention problem that existed in the conventional DCVS design. This leads PSLC to have lower power consumption and faster speed. Additionally, the proposed circuit can operate at different values of V_{DDL} ranging from 1.2V to 4.2V. From our simulation results, it is clear that both speed and power consumption of the proposed circuit are superior to those of existing circuit. Hence, the proposed technique is suited for low power design without degrading

performance.

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Table I: Comparison of two level converters (load=0.1pF)

Converter Schematic	VDDL (V)	VDDH (V)	Rise Time (ns)	Fall Time (ns)	Delay (ns)	Power Consumption (μW)	Power-Delay (ns-uw)
DCVS	4.2	5	0.3422	0.3752	0.7174	457.39	328.1316
	4	5	0.3537	0.3816	0.7353	454.34	334.0762
	3.8	5	0.3634	0.3894	0.7528	448.14	337.3598
	3.6	5	0.3761	0.4002	0.7763	444.68	345.2051
	3.4	5	0.3948	0.4104	0.8052	442.36	356.1883
	3.2	5	0.4149	0.4278	0.8427	441.39	371.9594
	3	5	0.4416	0.4496	0.8912	441.84	393.7678
	2.8	5	0.4752	0.4818	0.957	448.18	428.9083
	2.6	5	0.5238	0.5216	1.0454	455.02	475.6779
	2.4	5	0.5896	0.5865	1.1761	471.01	553.9549
	2.2	5	0.6880	0.6904	1.3784	496.46	684.3205
	2	5	0.8464	0.8834	1.7298	544.47	941.8242
	1.8	5	1.1484	1.3033	2.4517	648.51	1589.952
	1.6	5	1.8948	2.5104	4.4052	929.09	4092.827
	1.4	5	---	---	---	---	---
	1.2	5	---	---	---	---	---
PSLC	4.2	5	0.3385	0.4583	0.7968	433.30	345.2534
	4	5	0.3451	0.4601	0.8052	425.95	342.9749
	3.8	5	0.3539	0.4647	0.8186	419.33	343.2635
	3.6	5	0.3653	0.4702	0.8355	414.91	346.6573
	3.4	5	0.3793	0.4792	0.8585	412.62	354.2343
	3.2	5	0.3955	0.4892	0.8847	411.33	363.9037
	3	5	0.4158	0.5016	0.9174	409.71	375.868
	2.8	5	0.4419	0.5161	0.958	410.25	393.0195
	2.6	5	0.4736	0.5416	1.0152	411.62	417.8766
	2.4	5	0.5197	0.5736	1.0933	414.66	453.3478
	2.2	5	0.5844	0.6201	1.2045	420.79	506.8416
	2	5	0.6735	0.6898	1.3633	431.24	587.9095
	1.8	5	0.8172	0.8122	1.6294	454.41	740.4157
	1.6	5	1.0622	1.0457	2.1079	495.20	1043.832
	1.4	5	1.5550	1.6159	3.1709	591.64	1876.031
	1.2	5	3.031	3.779	6.8100	954.63	6501.030

使用於雙供應電壓之低功率位準轉換器設計

余 建 政

摘 要

在多供應電壓(MSV)電路中，位準轉換器佔很重要的地位。CMOS 邏輯電路中，需要特別的電路將低位準電壓轉換成高位準電壓。本文中，我們提出具低電壓、低功率消耗的位準轉換器；同時，我們和傳統的位準轉換電路 DCVS 做比較。經由 HSPICE 模擬數據可知：我們所提出的電路比傳統的位準轉換電路加快 60%的速度且減少 50%的功率損耗。因此，我們所提出的電路適合使用在 MSV、IO 緩衝器等高速、低功率消耗的應用上。

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