具輸出級之電壓峰值檢知器

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摘要

本文提出一種新穎架構之電壓峰值檢知器，其係由一差動放大器、一充電電晶體、一電容器C以及一輸出級所組成，其中，該差動放大器係做爲比較器使用，該充電電晶體係做爲充電器使用，用以提供電容器C 所需之充電電流，而該輸出級則用以調整該電容器C上之電壓信號V(C)，以便精確地輸出該輸入信號之峰值電壓本文所提出之電壓峰值檢知器，不但能精確地檢測出輸入信號之峰值電壓，並且兼具電路結構簡單、佔用的晶片面積小以及有利於裝置之小型化等多重功效，同時亦設置有輸出級以便有效防止因外部電路之擷取動作而遭致破壞所保持之輸入峰值電壓。

關鍵字：電壓峰值檢知器、差動放大器 、比較器

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Peak Voltage Detector with Output Stage

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Abstract

This paper introduces a newly-designed peak voltage detector, which consists of a differential amplifier, a charge transistor, a capacitor, and an output stage. In which, the differential amplifier serves as a comparator, the charge transistor is a charger for supplying the capacitor with the needed charge current, and the output stage shifts the voltage signal on the capacitor to provide a precise peak voltage of an input signal. The peak voltage detector in this paper can accurately measure the peak voltage of an input signal and also comes up with advantages like simple circuit design, minimal chip space, and suitable for use with smaller devices. In addition, the inclusion of an output stage can further prevent the held peak voltage disruption resulted from the accessing activities of the outer circuits.

Key Words：Peak voltage detector, Differential amplifier, Comparator.

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I. Introduction

For various applications, the peak voltages of an input signal must be measured and kept in the form of a direct current for following uses and analyses. The peak values for a series of impulses are usually more useful than those of averages, such as it is necessary to track and record the held peak value in the case of a qualitative test; the peak voltage detector is also required in the applications like measuring the attenuation of a voltage signal in transmission medium, A/D converter, maximum likelihood decoding system, and so on.

Until today, numerous peak voltage detection technologies, proposed by Robert and Frederick (1991), David (1994), Ericson et al. (1995), Ozguc (1996),Shinozaki et al. (1996),Smith(1998),Assadian et al. (1999), Lee et al. (2000),Wight et al. (2000),and Chen et al. (2002), had been brought to our attentions for accurate detection of the peak voltage of the input signal. But most of these peak voltage detectors have more than one operational amplifier, which translates into disadvantages like complex circuit design, larger chip space, and so on.

Lately, there emerged several precise peak voltage detection technologies proposed by Shiau et al. (2003) and Shiau (2003). For these technologies, the operational amplifier was replaced by the circuit consisting of a differential amplifier and a current mirror; and without the operational amplifiers, the technologies also had effects of simple circuit design, minimal chip space, and good for use with smaller devices. However, there was room for improvements in the number of transistors because the differential amplifier employed two load transistors and an independent current mirror was used. In addition, the peak voltage detectors did not equip with an output stage; the output stage can effectively maintain the held peak voltage during the accesses from outer circuits, and protect it from dropping or even destroyed due to any outer accessing activities.

The peak voltage detector in this

paper can accurately measure the peak voltage of an input signal and also comes up with advantages like simple circuit design, minimal chip space, and is good for use with smaller devices. In addition, the inclusion of an output stage can further prevent the held peak voltage disruption resulted from the accessing activities of the outer circuits.

The proposed peak voltage detector consists of a differential amplifier, a charge transistor, a capacitor, and an output stage. The differential amplifier is designed to be a non-symmetrical structure, i.e., only one-sided load transistor is used in the differential amplifier, and the load transistor and the charge transistor together constitute a current mirror; therefore, two lesser PMOS transistors in this new design than those of the traditional precision peak voltage detectors proposed by Shiau et al. (2003) and Shiau (2003) can be obtained. In addition, the proposed peak voltage detector has been equipped with an output stage, not only the held peak voltage can be protected from destruction through outer circuit access but also the input peak voltage can be accurately shifted and outputted.

II. Design Procedure

The proposed peak voltage detector is shown in Fig. 1; it consists of a differential amplifier, a charge transistor, a capacitor, and an output stage. The differential amplifier is designed with non-symmetrical circuit configuration, which comprises the NMOS transistors MN1, MN2, MN3, and the PMOS transistor MP1. Within which, the NMOS transistors MN1 and MN2 work as drivers while the PMOS transistor MP1 acts as the load transistor and the NMOS transistor MN3 provides a reference current to the differential amplifier. The gates of the NMOS transistors MN1 and MN2 receive respectively the input signal V(IN) and the voltage signal V(C) on the capacitor, and the sources of them connect together, then connected to the drain of the NMOS transistor MN3. And the drains of them connect respectively to load transistor MP1 and power supply voltage Vdd. In

addition, the gate of the NMOS transistor MN3 connects to power supply voltage Vdd and its source is grounded.

Let's refer back to Fig. 1 again, the load transistor MP1 and the charge transistor MP2 together form a current mirror, the sources of both PMOS transistors MP1 and MP2 are connected to the power supply voltage Vdd, their gates are connected together to the drain of the NMOS transistor MN1, and the gate and drain of the PMOS transistor MP1 are connected together to act as a diode. Furthermore, the drain of the PMOS transistor MP2 is connected to one side of the capacitor C while the other side is grounded. In addition, the output stage is formed by a NMOS transistor MN4 and a resistor R while it is connected between the power supply voltage Vdd and the ground.

For simplicity, the following derivation is based on the MOSFET Level 1 model, which is the simplest model, and neglects the channel length modulation effect. However, the all SPICE parameters for a MOS transistor in the MOSFET Level 3 model will be considered in the following simulations and verifications.

It can be seen from Fig. 1 when an input voltage signal V(IN) is greater than the voltage signal V(C) on the capacitor, the current Id(MN1) will be greater than the Id(MN2), and

$$Id(MN1) + Id(MN2) = Id(MN3) \quad (1)$$

And,

$$Id(MN1) = -Id(MP1) \quad (2)$$

Because the PMOS transistors MP1 and MP2 together forms a current mirror, we obtain

$$-Id(MP1) = -Id(MP2) \quad (3)$$

Thus, the PMOS transistor MP2 will charge the capacitor C. When the voltage signal V(C) on the capacitor equals to the peak voltage of an input voltage signal V(IN), then

$$Id(MN1) = Id(MN2) = 1/2\ Id(MN3) \quad (4)$$

The charge will still be performed to the capacitor C. Based upon the transfer characteristic of the differential amplifier, the voltage signal V(C) on the capacitor must be greater than the input peak voltage,

Vpeak, by the amount of overshoot voltage, Vos, for the NMOS transistor MN1 to be forced entering the cut-off region. When the NMOS transistor MN1 is in the cut-off region, the charge transistor will stop charging the capacitor C. And at this particular moment, the voltage signal V(C) on the capacitor is equal to

$$V(C) = V_{peak} + Vos \quad (5)$$

At this particular moment, the NMOS transistor MN2 is operating in the saturation region and the NMOS transistor MN1 is just entering the cut-off region from the saturation region. Hence, we can derive the gate-source voltage, VGS2, of the NMOS transistor MN2 and the gate-source voltage, VGS1, of the NMOS transistor MN1 from the following equations:

$$Id\ (MN2) = Id\ (MN3) \quad (6)$$

$$Id\ (MN1) = 0 \quad (7)$$

Therefore, the overshoot voltage Vos can be expressed as

$$Vos = VGS2 - VGS1 \quad (8)$$

After that, the voltage signal V (IN) drops from the peak voltage Vpeak and the NMOS transistor MN1 had entered the cut-off region, therefore the current

$$-Id\ (MP1) = -Id\ (MP2) = 0 \quad (9)$$

The charge transistor will not charge the capacitor C and the voltage signal V(C) on the capacitor will be fixed to the voltage in equation (5).

If all the NMOS transistors MN1, MN2 and MN3 in the differential amplifier have the same zero-bias threshold voltage VTO and transconductance parameter KP, we can refer to the book by Laker et al. (1994) and rewrite equation (8) as

$$Vos=[2 \cdot Id(MN3) \cdot 1/KP \cdot 1/(W/L)_{MN2}]^{1/2} \quad (10)$$

In which (W/L)MN2 is the aspect ratio of the NMOS transistor MN2. Note that the NMOS transistor MN3 is operating in the saturation region. The overshoot voltage Vos can thus be given by

$$Vos= [(W/L)_{MN3} /(W/L)_{MN2}]^{1/2} \cdot (Vdd - V_{TO}) \quad (11)$$

In which (W/L)MN3 is the aspect ratio of the NMOS transistor MN3.

Please refer back to Fig. 1, as the voltage signal V(C) on the capacitor is

lessened by a gate-source voltage, VGS4, of the NMOS transistor MN4, it becomes the output voltage signal V(OUT) of the peak voltage detector, that is

$$V(OUT) = V(C) - VGS4 \quad (12)$$

Next, from the equations (5) and (12), we can see if the output voltage signal V(OUT) is equal to input peak voltage Vpeak, there must be

$$VGS4 = Vos \quad (13)$$

That is the amount of the voltage shifted by the output stage. Lastly, it is known that the drain current Id (MN4) of NMOS transistor MN4 is a function of the gate-source voltage VGS4 , the drain-source voltage VDS4, and its aspect ratio (channel width to length ratio) and threshold voltage, therefore the output stage can be easily designed if the aspect ratio as well as the threshold voltage of the NMOS transistor MN4 and the resistance value r of resistor R are carefully chosen and satisfied the following equation:

$$(Vdd - VDS4)/r = Id(MN4) \quad (14)$$

By virtue of the above design procedures, we are able to design the peak voltage detector with relative ease. Sometimes the resistance value of the resistor R is significantly large greater than 50 mega-ohm and the aspect ratios of the NMOS transistor MN4 is selected more than a factor of ten. Thus, the zero-bias threshold voltage, V_{TO4}, of the NMOS transistor MN4 is a satisfactory approximation for the gate-source voltage, VGS4, of the NMOS transistor MN4. In this case, the relationship equation (13) can be rewritten as

$$V_{TO4} = [(W/L)_{MN3} / (W/L)_{MN2}]^{1/2} \cdot (Vdd - V_{TO}) \quad (15)$$

This reveals an alternate design of the peak voltage detector with less current consumption in the output stage.

III. Simulation and Verification

The simulation results from OrCAD PSpice transient analysis for the proposed peak voltage detector are shown in Figs. 2 to 6, based on the simulations under 0.35-μm CMOS technology, in which the aspect ratios of the NMOS transistors

MN1, MN2 and PMOS transistors MP1, MP2 are 0.35 μm:0.35 μm, the NMOS transistor MN3 is 0.35 μm:0.35 μm *30, all PMOS transistors and NMOS transistors have, respectively, -0.5V and 0.5V zero-bias threshold voltage, and the capacitance of capacitor is 1pF. From Figs. 2 to 4, it can be seen that the output voltage signal V(OUT) do only change by an amount of 1.5% even when the resistance value of the resistor in the output stage changed by 25%, this owing to the provided effective negative feedback from the resistor to the output voltage signal V(OUT).

From Figs. 2 and 5, it can also be seen that they almost have the same output voltage signal V(OUT) by increasing the resistance value of the resistor R from 1Meg ohm to 2Meg ohm and lowing the aspect ratio of NMOS transistor MN4 from 25*0.35 μm:0.35 μm to 12.5*0.35 μm : 0.35 μm, and then verify the result of equation (14). And Fig. 6, on the other hand, is the simulation result of OrCAD PSpice transient analysis when the input voltage signal V(IN) is of sinusoid waveform.

Figs. 7 and 8 show the simulation results of an alternate design of the peak voltage detector with less current consumption in the output stage, in which the aspect ratio of the NMOS transistor MN1 is 0.35 μm:0.35 μm, the NMOS transistor MN2 is 10*0.35 μm:0.35 μm, the NMOS transistor MN3 is 0.35 μm:0.35 μm*5, the NMOS transistor MN4 is 10*0.35 μm:0.35 μm, the PMOS transistors MP1 and MP2 are 2*0.35 μm:0.35 μm,all PMOS transistors and NMOS transistors but MN4 have, respectively, -0.5V and 0.5V zero-bias threshold voltage, the capacitance of capacitor is 0.01pF, and the power supply voltage is in the order of 5 Volts. From Figs. 7 and 8, it can also be seen that they have the same output voltage signal V(OUT) even the resistance value of the resistor R changed from 50 mega-ohm to 80 mega-ohm, and then the result of equation (15) can be verified.

From the above analyses, it is shown that the proposed peak voltage detector can

accurately and effectively measure the peak voltage in the input voltage waveform.

IV.Conclusions and Discussions

A differential amplifier, a charge transistor, a capacitor, and an output stage constitute this newly designed peak voltage detector introduced in this paper. It only uses two PMOS and four NMOS transistors, one capacitor, and one resistor. The peak voltage detector in this paper can accurately measure the peak voltage of an input signal and also comes up with advantages like simple circuit design, minimal chip space, and less number of transistors. In the mean time, it is also high integration because it doesn't need any operational amplifier. Additionally, the inclusion of an output stage can not only further prevent the held peak voltage disruption resulted from outer circuit access but also accurately shift the input peak voltage. Though the included output stage tends to limit the swing of an input voltage signal , it can be improved by using appropriate back-gate forward bias for the NMOS transistor MN4.

Nomenclature

Id (Mj)	drain current of the transistor Mj
KP	transconductance parameter for a MOS transistor in SPICE
r	the resistance value of the resistor R
Vdd	power supply voltage
Vos	overshoot voltage
V_{peak}	input peak voltage
V_{TO}	zero-bias threshold voltage for a MOS transistor in SPICE
V_{TO4}	zero-bias threshold voltage of the NMOS transistor MN4
V(C)	voltage signal on the capacitor
	VGSj gate-source voltage of the NMOS transistor MNj
VDSJ	drain-source voltage of the NMOS transistor MNj
(W/L)	the aspect ratio for a MOS transistor
$(W/L)_{MNj}$	the aspect ratio of the NMOS transistor MNj

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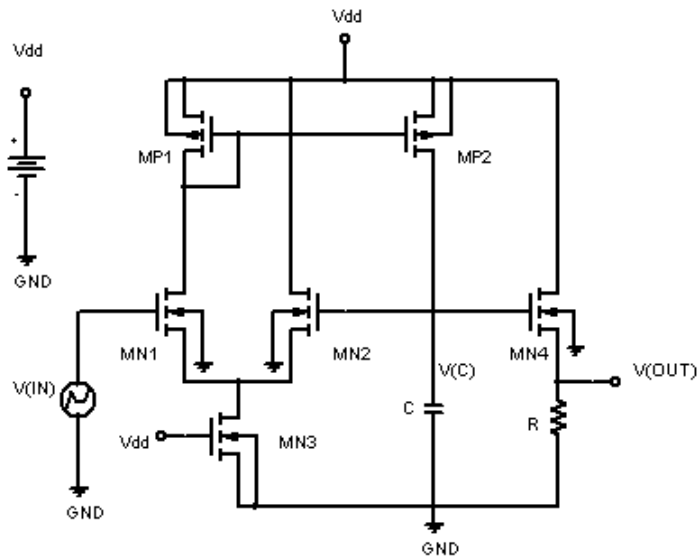

Fig. 1 Peak voltage detector structure.

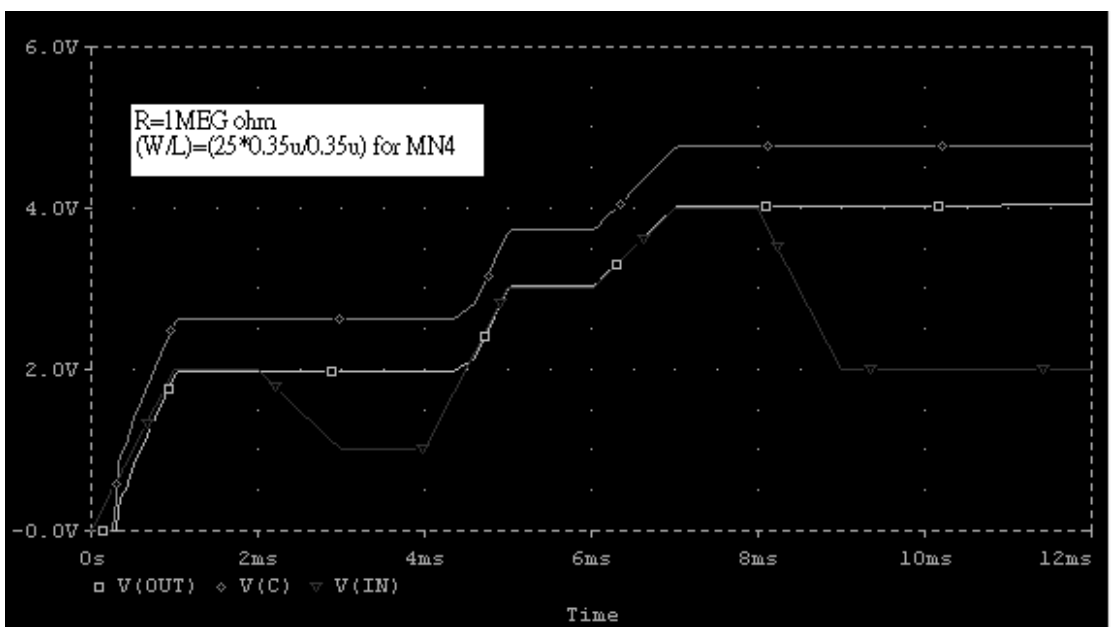

Fig. 2 Simulation result.(R=1 mega-ohm, $(W/L)_{MN4}$=25*0.35μm/0.35μm)

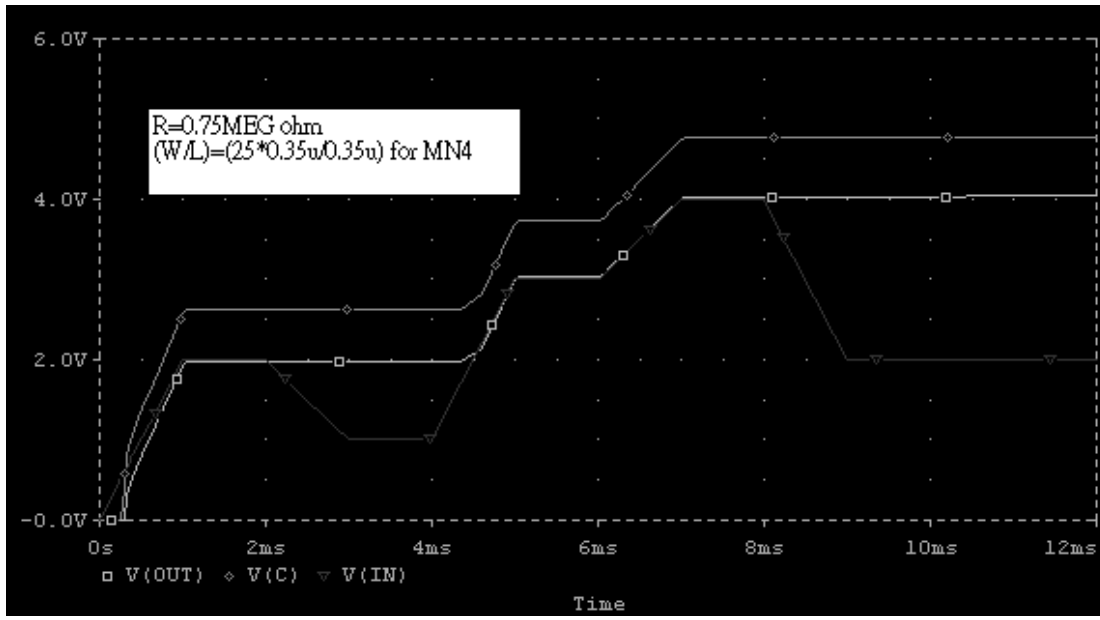

Fig. 3 Simulation result.(R=0.75 mega-ohm, $(W/L)_{MN4}$=25*0.35μm/0.35μm)

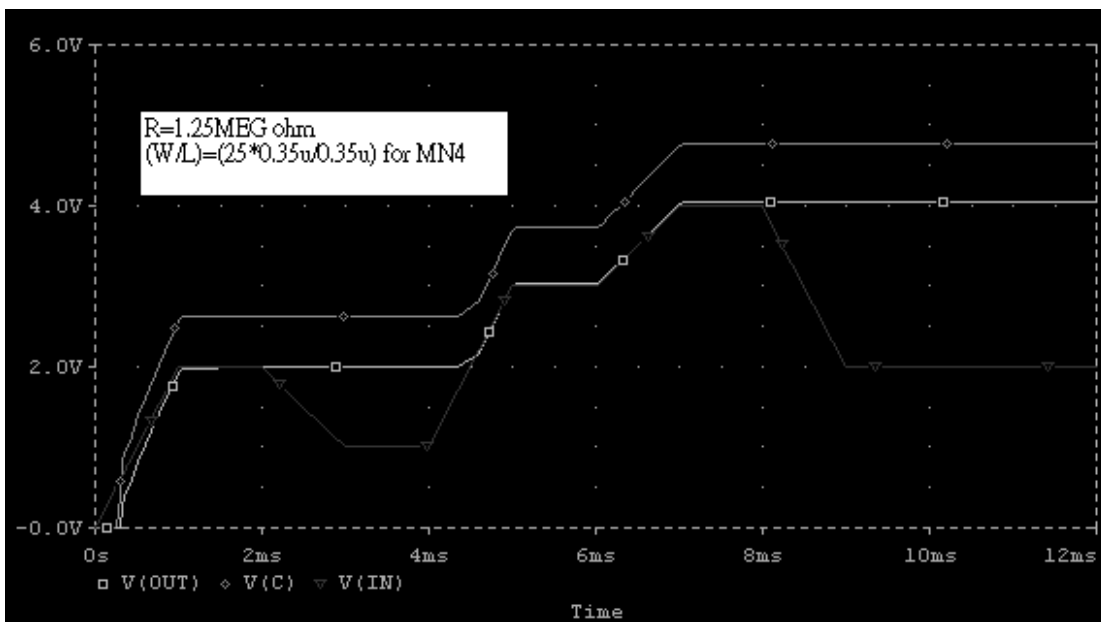

Fig. 4 Simulation result.(R=1.25 mega-ohm, $(W/L)_{MN4}$=25*0.35μm/0.35μm)

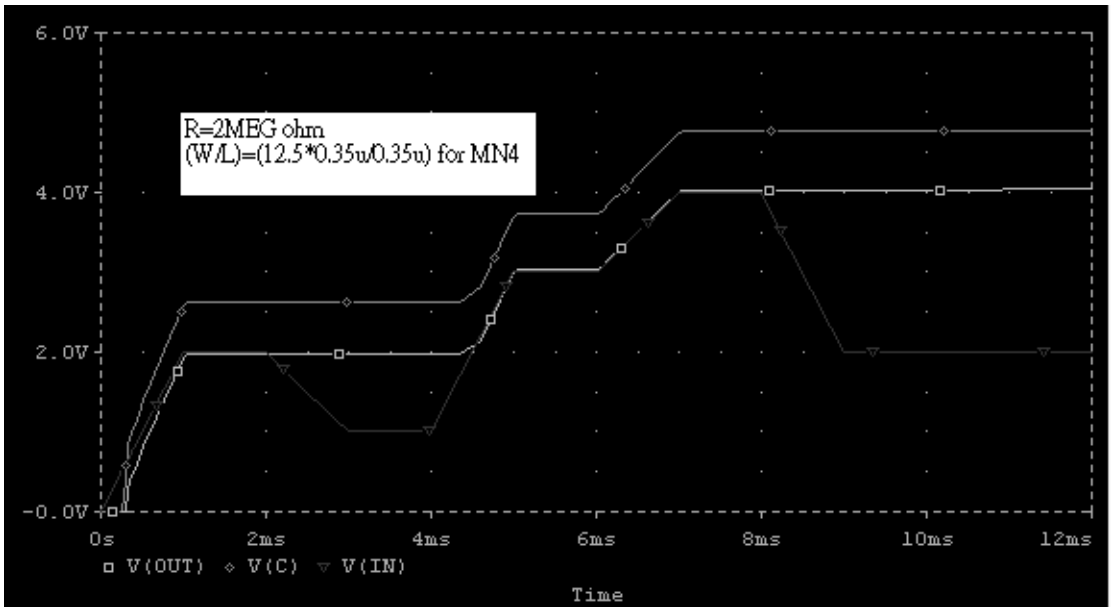

Fig. 5 Simulation result.(R=2 mega-ohm, $(W/L)_{MN4}$=12.5*0.35μm/0.35μm)

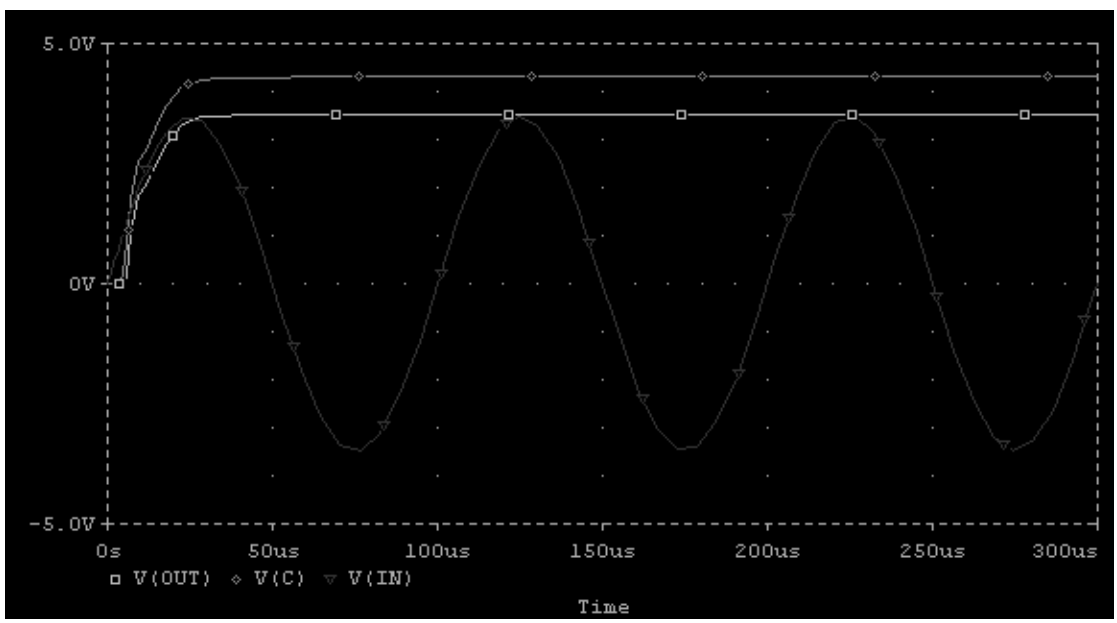

Fig. 6 Simulation result of sinusoid waveform. (R=1 mega-ohm, $(W/L)_{MN4}$= 25*0.35μm/0.35μm)

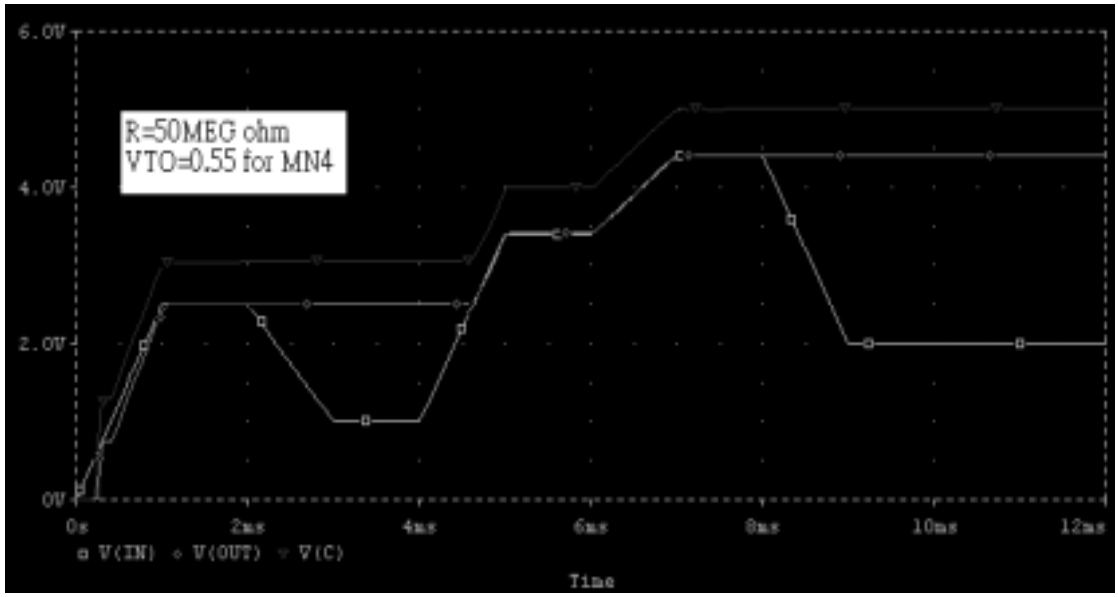

Fig. 7 Simulation result of the alternative design.(R=50 mega-ohm, V_{TO4} =0.55)

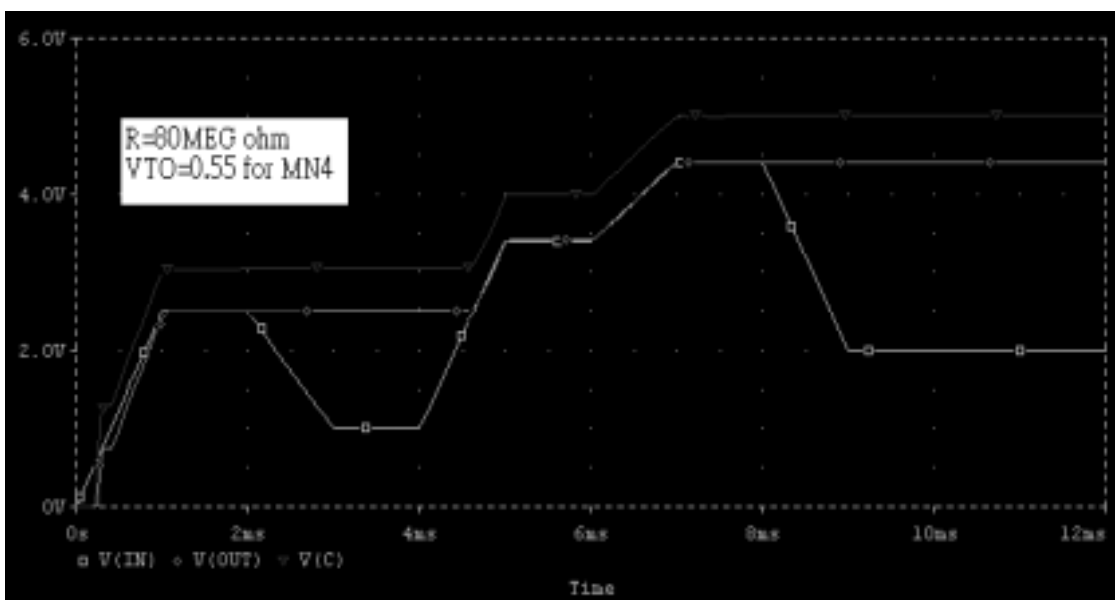

Fig. 8 Simulation result of the alternative design. (R=80 mega-ohm, V_{TO4} =0.55)